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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,369	06/13/2005	Geoffrey F Burns	US02 0543 US	6028

65913 7590 07/31/2008
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EXAMINER

PETRANEK, JACOB ANDREW

ART UNIT	PAPER NUMBER
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2183

NOTIFICATION DATE	DELIVERY MODE
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07/31/2008

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No. 10/538,369	Applicant(s) BURNS ET AL.	
	Examiner Jacob Petranek	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 June 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4-8,13,15-18 and 20-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,4-8,13,15-18 and 20-25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-2, 4-8, 13, 15-18, and 20-25 are pending.
2. The office acknowledges the following papers:
Claims, drawings, and arguments filed on 6/23/2008.

Withdrawn objections

3. The claim objection to claim 1 is withdrawn due to amendment.
4. The drawing objections to claims 11-12 and 14 are withdrawn due to cancellation of the claims.
5. The drawing objection for claim 1 is withdrawn due to the drawing amendments.

Claims objections

6. Claims 1 and 24-25 are objected to for the following reasons.
7. Claims 1 and 24-25 recite "the I/O pads." The limitation "input/output pads" should be changed to "input/output (I/O) pads" to clarify for antecedent basis purposes.

Maintained Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claim 20 is rejected under 35 U.S.C. §103(a) as being unpatentable over Fleck et al. (U.S. 6,434,689), in view of Roussakov (U.S. 6,092,174).

10. As per claim 20:

Fleck disclosed a method for interfacing a coprocessor to a main processor (Fleck: Figure 1 elements 7 and 4c, column 3 lines 19-28)(Figure 1 shows a coprocessor connected to a processor via interface element 7. The elements above the interface are the processor.), comprising the steps of:

communicatively connecting the coprocessor to said processor by an interface module (Fleck: Figure 1 elements 7 and 4c, column 3 lines 19-28)(Figure 1 shows a coprocessor connected to a processor via interface element 7. The elements above the interface are the processor.).

Fleck failed to teach configuring the coprocessor to compromise a two-dimensional array of processing cells and to have an execution speed greater than that of said processor and communicatively connecting the coprocessor to said processor by an interface module having a mechanism for reconfiguring a plurality of information paths between the interface module and respective cells on a periphery of the array.

However, Roussakov disclosed configuring the coprocessor to compromise a two-dimensional array of processing cells (Roussakov: Figure 1 element 1, column 5 lines 20-33.) and to have an execution speed greater than that of said processor (Roussakov: Column 3 lines 3-7)(The FPGA is able to be optimized to perform computer operations and is faster than computer processors. The processor of Fleck is

considered one of the computer processors mentioned by Roussakov and thus is slower than the FPGA.); and

an interface module having a mechanism for reconfiguring a plurality of information paths between the interface module and respective cells on a periphery of the array (Roussakov: Figure 3 elements 17 and 18, column 7 lines 1-24)(The limitations broadest reasonable interpretation is reconfiguring a plurality of information paths between the processing cells and the interface module. The FPGA allows for reconfigurations of data paths between the microcomputer modules, which are between the processing cells and the interface. The data paths transmit information and are therefore considered information paths. It's obvious to one of ordinary skill in the art that the reconfiguration mechanisms can be moved to the network interface. In addition, according to "In re Japikse" (181 F.2d 1019, 86 USPQ 70 (CCPA 1950)), shifting the location of parts doesn't give patentability over prior art.).

Fleck disclosed using a FPGA as part of the coprocessor of the system, but failed to disclose the details of the FPGA. Fleck also disclosed that the advantage of using FPGA's allows for benefits from being able to re-program them to perform specific tasks (Fleck: Column 4 lines 18-40). One of ordinary skill in the art would have been motivated by the lack of information by Fleck on FPGA's to add the functionality of Roussakov. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the FPGA of Roussakov into the processor of Fleck for the advantage of detailing the functionality of the FPGA of Fleck.

New Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claims 1, 5-8, 13, 15-16, and 21-23 are rejected under 35 U.S.C. §103(a) as being unpatentable over Higuchi et al. (U.S. 5,822,605).

13. As per claim 1:

Higuchi disclosed a coprocessor coupled to a main processor having an execution speed greater than that of said processor (Higuchi: Figure 1 elements 100 and 140, column 8 lines 33-50)(Element 140 is the main processor and all of the processing element (100) combined make up the coprocessor. It's obvious to one of ordinary skill in the art that the coprocessor is faster executing instructions than the host processor.), the coprocessor comprising a two-dimensional array of processing cells (Higuchi: Figure 1 element 100)(The processing elements make up a 2-d array.), including a plurality of periphery cells located on peripheral sides of the array (Higuchi: Figure 3 elements 30-32 and 303-305); and

an interface module (Higuchi: Figure 1 elements 116 and 132-139), comprising:

a plurality of input/output pads for the coprocessor (Higuchi: Figure 3 elements 30-32, column 14 lines 11-15)(Element 30 is an output pad for the processing element and elements 31-32 are input pads for the processing

element. There are pluralities of these elements because elements 30-32 are replicated for each processing element.),

a plurality of border cells disposed along an outside of the two-dimensional array, each border cell being connected to a corresponding one of the periphery cells, each border cell including a buffer (Higuchi: Figure 3 element 305, column 15 lines 8-16)(Output port buffers data being input to a processing element.), and

a crossbar network for reconfigurably connecting each of the I/O pads to one of the border cells (Higuchi: Figures 1 and 3 elements 132-139 and 310, column 8 lines 33-40 and 15 lines 1-7).

14. As per claim 5:

Higuchi disclosed inter-cell connection within the array is such that each cell of the array is connected only to cells whose column is the same and whose row is immediately adjacent, and only to cells whose row is the same and whose column is immediately adjacent (Higuchi: Figures 1 and 3 elements 132-139 and 310, column 8 lines 33-40 and column 15 lines 1-7)(Official notice is given that the 2-D array can be configured to limit processing element message passing to the nearest neighbor elements. Thus, it's obvious to one of ordinary skill in the art that processing element message passing is limited to the processing element's nearest neighbors.).

15. As per claim 6:

Higuchi disclosed the coprocessor of claim 1, wherein the coprocessor interface module and main processor of claim 1 and a shared memory that communicatively

connects with the interface module and the main processor to provide the main processor to coprocessor connection (Higuchi: Figure 1 elements 100 and 140, column 8 lines 33-50)(Official notice is given that the host processor and coprocessor 2-D array can have a shared memory among themselves to store data. Thus, it's obvious to one of ordinary skill in the art that the host processor and coprocessor share a memory.).

16. As per claim 7:

Higuchi disclosed the coprocessor of claim 1, including an array processor that comprises said two-dimensional array (Higuchi: Figure 1 elements 100 and 140, column 8 lines 33-50)(All of the processing elements (100) combined make up the 2-D array.).

17. As per claim 8:

Claim 8 essentially recites the same limitations of claim 1. Therefore, claim 8 is rejected for the same reasons as claim 1.

18. As per claim 13:

Higuchi disclosed a functional unit having a two-dimensional array of processing cells and being coupled to a main processor (Higuchi: Figure 1 elements 100 and 140, column 8 lines 33-50)(Element 140 is the main processor and all of the processing element (100) combined make up the coprocessor.), the unit having a mechanism external to the two-dimensional array for reconfiguring a plurality of intra-processor information paths to the array to respective cells on a periphery of the array (Higuchi: Figures 5-6 elements 504-507 and 705, column 15 lines 54-61 and column 16 lines 31-54)(The crossbar control is external to the 2-D array and reconfigures the message paths through controlling the switches connecting processing elements.).

19. As per claim 15:

The additional limitation(s) of claim 15 basically recite the additional limitation(s) of claim 5. Therefore, claim 15 is rejected for the same reason(s) as claim 5.

20. As per claim 16:

Higuchi disclosed the unit of claim 13, further including means for transmitting a plurality of array programs to corresponding predetermined subsets of said processing cells (Higuchi: Figure 1 elements 116 and 132-139)(The exchange and crossbar elements are able to transmit data to the processing elements.).

21. As per claim 21:

Higuchi disclosed the coprocessor of claim 1, wherein the array is rectangular (Higuchi: Figure 1 elements 100)(The array of processing elements is square. However, it's obvious to one of ordinary skill in the art that the array can be expanded in size to result in a rectangular shape. In addition, according to "In re Japikse" (181 F.2d 1019, 86 USPQ 70 (CCPA 1950)), shifting the location of parts doesn't give patentability over prior art.), wherein the periphery consists of those of said processing cells located in all of a first row, last row, first column and last column of said array (Periphery by definition is the boundary of an area (The American Heritage Dictionary of the English Language, Fourth Edition), therefore the periphery of the array is inherently the first row, last row, first column and last column.), and wherein the interface module's mechanism for reconfiguring a plurality of information paths reconfigures information paths directly connecting the interface module and each of the cells on the periphery of the array

(Higuchi: Figures 1 and 3 elements 132-139 and 310, column 8 lines 33-40 and 15 lines 1-7)(The crossbar network allows for reconfiguring paths within the 2-D array.).

22. As per claim 22:

Higuchi disclosed the coprocessor of claim 1, wherein the interface comprises a plurality of border cells directly connected to the respective processing cells on the periphery of the array (Higuchi: Figure 3 element 305, column 15 lines 8-16)(Output port buffers data being input to a processing element.).

23. As per claim 23:

Higuchi disclosed the coprocessor of claim 1, further comprising a master cell for forwarding array programs to the processing cells of the two-dimensional array (Higuchi: Figure 1 element 140, column 8 lines 44-50)(The host processor is the master cell that loads programs to the 2-D array.).

24. As per claim 24:

The additional limitation(s) of claim 24 basically recite the additional limitation(s) of claim 1. Therefore, claim 24 is rejected for the same reason(s) as claim 1.

25. Claim 2 is rejected under 35 U.S.C. §103(a) as being unpatentable over Higuchi et al. (U.S. 5,822,605), further in view of Miyamori et al. ("REMARC: Reconfigurable multimedia array coprocessor").

26. As per claim 2:

Higuchi disclosed the coprocessor of claim 1.

Higuchi failed to teach the array comprises a systolic processing array.

However, Miyamori discloses the array comprises a systolic processing array (Miyamori: Figure 2, page 396 column 1 paragraph 2).

The advantage of arranging a reconfigurable architecture in a systolic manner is that it can exploit fine-grained parallelism and achieve higher performance versus other multimedia extensions (Miyamori: Page 389 column 2 paragraph 2). One of ordinary skill in the art would have been motivated by this advantage to allow for systolic processing on the processing array of Higuchi. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement systolic processing on the array of Higuchi to gain increased performance by exploiting fine-grained parallelism.

27. Claims 4 and 17-18 are rejected under 35 U.S.C. §103(a) as being unpatentable Higuchi et al. (U.S. 5,822,605), further in view of Barat et al. ("Reconfigurable instruction set processor: An implementation platform for interactive multimedia applications").

28. As per claim 4:

Higuchi disclosed the coprocessor of claim 1.

Higuchi failed to teach wherein the coprocessor performs mathematical operations whose timing is based on a flow of input operands along the paths.

However, Barat disclosed wherein the coprocessor performs mathematical operations whose timing is based on a flow of input operands along the paths (Barat: Page 484 column 1 paragraph 2)(The compiler generates code with timing delays of the processing elements and interconnects in mind. Official notice is given that instructions

executed on a processor can include mathematical operations that use operands.

Thus, it's obvious to one of ordinary skill in the art that the instructions executed are mathematical operations that use operands.).

The advantage of the reconfiguration method of Barat is that it allows for a compiler to more efficiently execute loops by storing configurations locally (Barat: Page 483, section 2.2 paragraph 2). One of ordinary skill in the art would have been motivated by this advantage to implement it within the processor of Higuchi. Thus, one of ordinary skill in the art at the time of the invention would have implemented the reconfiguration method of Barat into the processor of Higuchi for the advantage of more efficiently executing loops.

29. As per claim 17:

Higuchi disclosed a system including the functional unit of claim 16.

Higuchi failed to teach an array program generator for generating the array programs to be transmitted, and, when needed, updating a program, transmitting the updated program, and transmitting concurrently, when needed, a reconfigure signal to said mechanism to correspondingly update a current steady state connection pattern of said information paths.

However, Barat disclosed an array program generator for generating the array programs to be transmitted (Barat: Page 483, section 2.2 paragraph 2)(The compiler generates programs executed on the array of Higuchi.), and, when needed, updating a program, transmitting the updated program, and transmitting concurrently, when needed, a reconfigure signal to said mechanism to correspondingly update a current

steady state connection pattern of said information paths (Barat: Page 483, section 2.2 paragraph 1)(The ROP field will be a signal to update the reconfigurable microcomputer clusters of Higuchi to be able to execute an instruction. The instruction that is executed is also transferred to the array to be executed.).

The advantage of the reconfiguration method of Barat is that it allows for a compiler to more efficiently execute loops by storing configurations locally (Barat: Page 483, section 2.2 paragraph 2). One of ordinary skill in the art would have been motivated by this advantage to implement it within the processor of Higuchi. Thus, one of ordinary skill in the art at the time of the invention would have implemented the reconfiguration method of Barat into the processor of Higuchi for the advantage of more efficiently executing loops.

30. As per claim 18:

Higuchi and Barat disclosed the system of claim 17, further including a compiler configured for receiving, in response to said program updating data representative of input and output timing for said unit (timing delay) and further configured for compiling an instruction based on said data (Barat: Page 484 column 1 paragraph 2)(The compiler generates code with timing delays of the processing elements and interconnects in mind.).

31. Claim 25 is rejected under 35 U.S.C. §103(a) as being unpatentable over Fleck et al. (U.S. 6,434,689), in view of Roussakov (U.S. 6,092,174), further in view of Higuchi et al. (U.S. 5,822,605).

32. As per claim 25:

The additional limitation(s) of claim 25 basically recite the additional limitation(s) of claim 1. Therefore, claim 25 is rejected for the same reason(s) as claim 1.

The advantage of the 2-D array of Higuchi is that it allows for greater efficiency in message passing by allowing processing elements to route messages to any other processor in the array (Higuchi: Column 14 lines 11-19). One of ordinary skill in the art would have been motivated by this advantage to implement the crossbar network of Higuchi into the processor of Roussakov. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the crossbar network of Higuchi into the processor of Roussakov for the advantage of increased efficiency in message passing between processing elements.

Response to Arguments

33. The arguments presented by Applicant in the response, received on 6/23/2008 are partially considered persuasive.

34. Applicant argues "Fleck nor Roussakov disclosed the interface module comprising a plurality of I/O pads, a plurality of border cells, and a crossbar network" for claim 1.

This argument is found to be persuasive for the following reason. The examiner agrees that Fleck and Roussakov failed to teach the newly claimed limitations. However, a new ground of rejection has been given due to the amendment.

35. Applicant argues "Fleck nor Roussakov disclosed an external mechanism for reconfiguring a plurality of intra-processor information paths" for claim 13.

This argument is found to be persuasive for the following reason. The examiner agrees that Fleck and Roussakov failed to teach the newly claimed limitations.

However, a new ground of rejection has been given due to the amendment.

36. Applicant argues "Fleck nor Roussakov disclosed an interface module having a mechanism for reconfiguring a plurality of information paths between the interface module and respective cells on a periphery of the array" for claim 20.

This argument is not found to be persuasive for the following reason. The FPGA allows for reconfigurations of data paths between the microcomputer modules, which are between the processing cells and the interface. The data paths transmit information and are therefore considered information paths. It's obvious to one of ordinary skill in the art that the reconfiguration mechanisms can be moved to the network interface. In addition, according to "In re Japikse" (181 F.2d 1019, 86 USPQ 70 (CCPA 1950)), shifting the location of parts doesn't give patentability over prior art.).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Agrawal et al. (5,093,920), taught a processing array network.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Examiner, Art Unit 2183